We claim:

1. An electrically operated memory element, comprising:

a programmable resistance memory material; and

a conductive layer in electrical communication with said memory material, said conductive layer having a raised portion extending from an edge of said layer to an end adjacent said memory material.

2. The memory element of claim 1, wherein said raised portion tapers to said end adjacent said memory material.

3. The memory element of claim 1, wherein at least a portion of said conductive layer is substantially vertically disposed.

4. The memory element of claim 1, wherein at least a portion of said conductive layer is disposed on a sidewall surface.

5. The memory element of claim 4, wherein said sidewall surface is cylindrical.

6. The memory element is claim 4, wherein said sidewall surface is substantially flat.

7. The memory element of claim 1, wherein conductive layer is a conductive sidewall spacer.

8. The memory element of claim 1, wherein said conductive layer is a conductive liner.

9. The memory element of claim 7, wherein said conductive sidewall spacer is formed in a trench, via or mesa.

10. The memory element of claim 8, wherein said conductive liner is formed in a trench or via.

11. The memory element of claim 1, wherein said edge is an annulus.

12. The memory element of claim 1, wherein said edge is linear.

13. The memory element of claim 1, wherein said memory material and said conductive layer have an area of contact having an area less then 0.005 micron^2.

14. The memory element of claim 1, wherein said conductive layer is disposed on the sidewall surface and the bottom surface of a trench or via.

15. The memory element of claim 1, wherein said memory material is a phase-change material.

16. The memory element of claim 1, wherein said memory material comprises a chalcogen element.

17. An electrical contact for a semiconductor device, comprising:

an insulative layer;

an opening formed in said insulative layer, said opening having a sidewall surface and a bottom surface; and

a conductive layer disposed on said sidewall surface of said opening, said layer having a raised portion extending from an edge of said conductive layer on said sidewall surface.

18. The memory element of claim 17, wherein said conductive layer is disposed on said sidewall surface and said bottom surface of said opening.

19. The memory element of claim 17, wherein said opening is a trench or a via.

20. The memory element of claim 17, wherein said memory material is a phase-change material.

21. The memory element of claim 17, wherein said memory material includes at least on chalcogen element.

22. A method for making a programmable resistance memory element, comprising:

providing a conductive layer;

forming a raised portion on an edge of said conductive layer; and

depositing a programmable resistance memory material adjacent said raised portion.

23. The method of claim 22, wherein said forming said raised portion comprises:

etching a portion of said conductive layer to form said raised portion.

24. A method for making a programmable resistance memory element, comprising:

providing a conductive sidewall layer;

forming a raised portion on an upper edge of said conductive layer; and

depositing a programmable resistance memory material adjacent said raised portion.

25. The method of claim 24, wherein said forming said raised portion comprises:

forming a spacer above said conductive layer;

using the spacer as a mask, etching said conductive layer to

form said raised portion below said spacer.

26. The method of claim 25, wherein said forming said spacer comprises:

depositing a first layer above said conductive layer;

depositing a second layer onto said first layer;

etching said second layer to form a sidewall surface;

depositing a third layer onto said sidewall surface;

27. The method of claim 26, further comprising:

after depositing said third layer,

anisotropically etching said third layer;

removing said second layer;

anisotropically etching said first layer.

28. The method of claim 26, wherein said first and said third layers comprise an oxide.

29. The method of claim 26, wherein said second layer comprises polysilicon.

30. The method of claim 26, wherein said first and third layers comprise a nitride.

31. The method of claim 26, wherein said second layer comprises an oxide.

32. An electrically operated memory element, comprising:

a programmable resistance memory material; and

a conductive layer in electrical communication with said memory material, said conductive layer having a raised portion extending from an edge of said layer wherein substantially all of the electrically communication occurs through said raised portion.

33. The memory element of claim 32, wherein said raised portion extends from said edge to a tip wherein substantially all of the electrical communication occurs through said tip.

34. The memory element of claim 32, wherein said raised portion tapers to said tip.

35. The memory element of claim 32, wherein at least a portion of said conductive layer is substantially vertically disposed.

36. The memory element of claim 32, wherein at least a portion of said conductive layer is a sidewall layer.

37. The memory element of claim 32, wherein conductive layer is a conductive sidewall spacer.

38. The memory element of claim 32, wherein said conductive layer is a conductive liner.

39. The memory element of claim 32, wherein said edge is an annulus.

40. The memory element of claim 32, wherein said edge is linear.

41. The memory element of claim 32, wherein said memory material and said conductive layer have an area of contact having an area less then 0.005 micron^2.

42. The memory element of claim 32, wherein said conductive layer is disposed on the sidewall surface and the bottom surface of a trench or via.

43. The memory element of claim 32, wherein said memory material is a phase-change material.

44. The memory element of claim 32, wherein said memory material comprises a chalcogen element.